IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Hildebrant

Serial No.: 10/736,438

Filed: 12/15/2003

Confirmation No.: 3423

Group Art Unit: 2112

Examiner: RIZK, Samir Wadie

Docket No. 10030775-1

For: **Systems and Methods for Adaptively Compressing Test Data**

STATEMENT OF FACTS UNDER C.F.R. §1.181(b) ACCOMPANYING PETITION TO WITHDRAW FINAL OFFICE ACTION AND REQUEST FOR ACTION

Mail Stop - Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Applicant hereby submits the following statement of facts:

Final Office Action

(1) a final Office Action (part of paper no./mail date 20070731) was mailed on August 7, 2007 (Exhibit A).

(2) on page 2, section 2 of the final Office Action (Response to Arguments Section), the following explanation is provided by the Examiner (no emphasis added):

> The Applicant emphasized the claimed features in amended claim 1:
> a) determining a timing complexity for the first plurality of data units;
> b) determining a timing complexity for the second plurality of data units;
> And, the Applicant goes on to explain that "Simply monitoring or evaluating data changes does not necessarily involve and determination as to timing complexity."
> Actually the Applicant has quoted Ishida in page 9, line 22-23 teaches **calculating** a threshold value of the number of data changes. The Examiner maintains that calculating is a means of determining the complexity of the data units as recited in amended claim 1.

(3) on page 3, section 3 of the final Office Action (Response to Arguments Section), the following explanation is provided by the Examiner (no emphasis added):

> In regard to claim 14, that is cancelled and the limitation has been incorporated into the independent claim 12, Examiners disagrees with the Applicant quotation of section [0061] in Wang to conclude in page 13, lines 29-31 if the applicant's remarks:
>
> "Neither the above-cited section of *Wang*, nor elsewhere in *Wang*, discloses, teaches, or suggests that the signals pertaining to the external scan input pins 111 and the external primary input pins 113 correspond to clock signals and non-clock signals, respectively."
>
> The Examiner re-iterates that Wang in FIG. 1, reference characters (110) and (113) teaches combinational logic test pins. Combinational logic is inherently non-clock signals to those of ordinary skill in the art. Also, Wang in FIG. 1, reference characters (108), (109) and (111) teaches SC "Scan Chain" test pins. Scan chain is inherently clock signals to those of ordinary skill in the art.

(4) on page 3, section 4 of the final Office Action (Response to Arguments Section), the following explanation is provided by the Examiner:

> The Examiner disagrees with the applicant and maintains the rejection of claims 1, 3-13, 15-17, 19-29, 31 and 32 as in the office action mailed on 3/16/2007. All the amendments and arguments have been considered. It is the Examiner's conclusion that claims 1, 3-13, 15-17, 19-29, 31 and 32 are not patentably distinct or non-obvious over the prior art of record in view of the reference, Ishida and Wang. Therefore the rejection is maintained.

(5) on page 4, section 2 of the final Office Action, claim 12 is among the claims listed as rejected under 35 U.S.C. 102(e) "as being anticipated by Ishida."

(6) on page 5, section 10 of the final Office Action, the following explanation is provided by the Examiner:

> 10. Claim 12 is rejected for the same reason as per claim 1.

(7) on page 6, section 19 of the final Office Action, the following explanation is provided by the Examiner:

19. Claim 28 is rejected for the same reasons as per claim 17.

(8) on page 6 of the final Office Action, claim 14 is among the claims listed as rejected under 35 U.S.C. 103(a) "as being unpatentable over Ishida as applied to claim 1 above, and further in view of Wang et al. US publication no. 2006/0242502."

Claims 1, 12, 14, 17, and 28 in the response preceding the final Office Action

(9) a response to the non-final Office Action dated March 16, 2007 was submitted to the USPTO on June 14, 2007 (Exhibit D).

(10) In the June 14, 2007 response, the following claims 1, 12, 17, and 28 were presented:

1. A method for adaptively compressing test data to be provided to a device under test (DUT), the method comprising the steps of:
examining a test data file that includes a first plurality of data units corresponding to a first plurality of DUT pins and a second plurality of data units corresponding to a second plurality of DUT pins;
determining a timing complexity for the first plurality of data units;
determining a timing complexity for the second plurality of data units;
compressing the first plurality of data units using a first compression technique; and
compressing the second plurality of data units using a second compression technique.

12. A method for adaptively compressing test data to be provided to a device under test (DUT), the method comprising the steps of:
examining a test data file that includes test data configured to enable testing the DUT, the test data file including a first plurality of data units and a second plurality of data units, the first plurality of data units corresponding to a first plurality of DUT pins, and the second plurality of data units corresponding to a second plurality of DUT pins, wherein the first plurality of DUT pins are clock-pins and the second plurality of DUT pins are non-clock-pins;
determining that the first plurality of data units have a first compressibility characteristic; and
determining that the second plurality of data units have a second compressibility characteristic.

17. A system for adaptively compressing test data to be provided to a device under test (DUT), the system comprising:
memory configured to store a test data file that includes a first plurality of data units corresponding to a first plurality of DUT pins and a second plurality of data units corresponding to a second plurality of DUT pins; and
a processor operative to:
determine a timing complexity for the first plurality of data units;
determine a timing complexity for the second plurality of data units;
compress the first plurality of data units using a first compression technique; and
compress the second plurality of data units using a second compression technique.

28. A system for adaptively compressing test data to be provided to a device under test (DUT), the system comprising:
memory configured to store a test data file that includes test data configured to enable testing the DUT, the test data file including a first plurality of data units and a second plurality of data units, the first plurality of data units corresponding to a first plurality of DUT pins, and the second plurality of data units corresponding to a second plurality of DUT pins, wherein the first plurality of DUT pins are clock-pins and the second plurality of DUT pins are non-clock-pins; and
a processor that is operative to:
determine that the first plurality of data units have a first compressibility characteristic;
determine that the second plurality of data units have a second compressibility characteristic.

(11) From the above claims, it is noted from a comparison of claims 1 and 12 that claim 1 does not include the feature of "wherein the first plurality of DUT pins are clock-pins and the second plurality of DUT pins are non-clock-pins" found in claim 12.

(12) From the above claims, it is noted from a comparison of claims 17 and 28 that claim 17 does not include the feature of "wherein the first plurality of DUT pins are clock-pins and the second plurality of DUT pins are non-clock-pins" found in claim 28.

(13) In the June 14, 2007 response, claim 14 was canceled.

After final response

(14) a response to the final Office Action dated August 7, 2007 was submitted to the USPTO on October 5, 2007 (Exhibit B).

(15) on page 4 of the above-referenced response to final Office Action, Applicant points out the confusion, stemming from the Examiner's allegation in the final Office Action [see (6) and (7) above] alleging claims 12 and 28 are rejected for the same reasons as claims 1 and 17, as follows:

> Applicant respectfully notes that the final Office action is confusing in that page 5 asserts that claim 12 "is rejected for the same reasons as per claim 1." Similarly, the final Office Action on page 6 alleges that claim 28 "is rejected for the same reasons as claim 17." However, Applicant respectfully notes that claims 1 and 17 lack the below-emphasized features found in claims 12 and 28, respectively, and that those emphasized features are not addressed in the rejection to claims 1 and 17.

(16) on page 4 of the above-referenced response to final Office Action, Applicant points out the confusion, as to whether the final rejection of claims 12 and 28 is based on 102(e) or 103(a) grounds, as follows:

> Additionally, the confusion is perpetuated by the fact that the "Response to Arguments" section on page 3 appears to attempt to address the arguments presented in support of patentability of claims 12 and 28 in Applicant's last response, but uses *Wang* and fails to address the explicit claim features. Accordingly, Applicant queries whether the rejection to claims 12 and 28 is based on 103(a) (*Ishida* and *Wang*), 102(e) (*Wang*), or 102(e) (*Ishida*).

(17) on pages 4 and 5 of the above-referenced response to final Office Action, Applicant requests reconsideration of the finality of the final Office Action pursuant to 37 C.F.R. 1.181(c) as follows:

> Further, Applicant respectfully submits that the failure to address the explicit claim features renders the rejection improper under MPEP 706 (e.g., 37 CFR 1.104), and hence Applicant respectfully requests that the next Office Action, if not a Notice of Allowance, be made non-final to accord Applicant an adequate opportunity to address any rejection of the explicit claim features and clarify issues for appeal.

Advisory action

(18) An Advisory Action dated October 19, 2007 (Part of paper no. 20071012) was mailed on October 19, 2007 (Exhibit C).

(19) The Advisory Action addresses Applicant's response after final as follows in the Continuation Sheet:

> 1. Applicant arguments in regard to claims 12 and 28 do not overcome the final rejection. The Examiner maintains that Wang teaches CLOCKED PINS as per the claims 12 and 28 language.
> 2. The Applicant is refered to section [0029] of the instant application and the disclosure of Wang in FIG. 1, reference characters (108) and (109) of CLOCKED PINS disclosure as in claims 12 and 28.
> 3. Claims amendments will be entered.

(20) Claims 12 and 28 do not contain the terms "CLOCKED PINS" as alleged in the Advisory Action [see (11) and (12) above for claim features].

Action requested

(21) Applicant respectfully requests that the Director intervene to address the ambiguity in the final Office Action and Advisory Action as to grounds of rejection and reasoning behind those grounds, to correct the Examiner's failure to address the explicit claim features (in the Advisory Action and in the final Office Action when a rejection to one claim is improperly applied to another (see (6) and (7) above)), and to remove the finality of the rejection. If any further information is required, Applicant requests that the USPTO contact the representative identified below at (770) 933-9500.

Respectfully submitted,

/dr/
David Rodack
Registration No. 47,034

THOMAS, KAYDEN,
HORSTEMEYER & RISLEY, L.L.P.
Suite 1750
100 Galleria Parkway N.W.
Atlanta, Georgia 30339
(770) 933-9500